Direct measurement of topography-dependent charging of patterned oxide/semiconductor structures

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Electron shading, or topography-dependent charging, occurs during plasma exposure of wafers with high-aspect-ratio features due to an imbalance between the electron and ion currents that reach the feature bottoms. High-aspect-ratio pit structures were exposed to an electron cyclotron resonance plasma. The surface potential of the structures after plasma exposure was measured with scanning surface-potential microscopy (SSPM). The results show that SSPM can be used to measure the differential charging in a high-aspect-ratio pit. *In situ* depletion of the plasma-induced charge with ultraviolet radiation was time resolved using SSPM. A circuit model is used to explain the experimental results. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2805023]

During plasma processing of semiconductor wafers with high-aspect-ratio surface features, differential charging occurs inside a high-aspect-ratio pit or trench due to the difference in the angular distribution between the ions and electrons reaching the pit bottom from the plasma.[1] The heavier and highly directional ions from the plasma are accelerated by the electric field in the sheath and the wafer bias so that they can easily reach the pit bottom. The electrons, due to their isotropic velocity distribution and lighter mass, come to rest on the sidewalls near the pit opening producing a local imbalance between ion and electron currents. This results in the pit bottom developing a positive potential. Eventually, a steady state is reached in which the ion and electron currents balance everywhere on the wafer and no further charging occurs.[1] This topography-dependent, plasma-induced charging mechanism is called electron shading[1] and is known to worsen with increasing aspect ratio of surface features,[1–3] decreasing feature size,[3] and increasing wafer bias.[4]

Electron shading is a serious problem in dielectric and metal/poly-Si etch processes that are routinely used in semiconductor processing. In metal-oxide-semiconductor devices, electron shading can introduce the Fowler-Nordheim tunneling currents[1] in thin gate dielectrics and thus degrade their quality. In addition, electron shading can also cause structural defects during etching in the form of sidewall bowing, microtrenching, and undercutting (notching).[1,5–7]

In this letter, we show direct measurements of electron shading. This is a challenging task because of the small dimensions and high-aspect ratio of the surface features. In the past, specialized test structures[8,9] were used to determine the presence or absence of electron shading indirectly by measuring localized currents.

For direct measurement of the surface potential produced by electron shading in patterned structures, an atomic force microscope with carbon nanotube tips is operated as a Kelvin probe[10] to spatially resolve the surface potentials of patterned structures on the microscale before and after plasma exposure. In addition, the same technique can be used to measure the surface-potential *in situ* during exposure of the test structures to ultraviolet (UV) radiation from a mercury-argon lamp. This technique also allows for measurements of the same location on the wafer before and after UV exposure.

The inset of Fig. 1 shows a scanning electron microscopy (SEM) image of the cross section of the test structures used. A 200-nm-thick oxide layer is thermally grown on top of etched Si to form a pit structure. The hole diameter and pitch were ~0.8 and 1.6 μm, respectively, for all structures. The sample (die) size was 8×8 mm^2. The pit depth was varied from 1 to 11 μm in order to study charging as a function of aspect ratio. In Fig. 1, the pit shown has a depth of 2 μm.

An electron cyclotron resonance (ECR) plasma was used to charge the patterned oxide-coated wafers. A helium ECR discharge at 20 mTorr was generated with 100 W of 2.45 GHz microwave radiation. Samples with different aspect ratio (AR) were exposed to the plasma simultaneously for approximately 30 s. The wafer substrates were secured to the wafer chuck by conductive silver paint and grounded to the chamber through conductive carbon tape. Spatially resolved measurements of the surface potential of the wafers

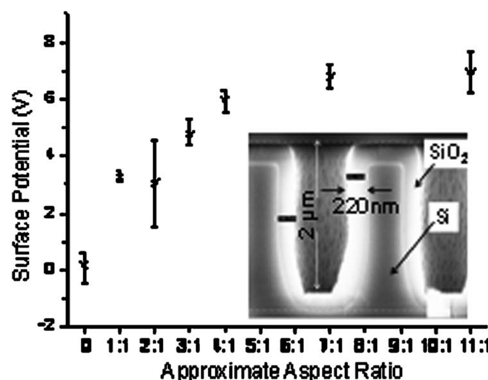

FIG. 1. Dependence of the average surface potential as a function of the aspect ratio of the pits. The inset shows the SEM image of the cross section of a sample patterned wafer with an aspect ratio of ~2.5:1.

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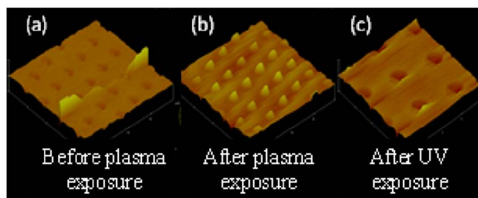

FIG. 2. (Color online) Two-dimensional surface maps (8×8 μm^2) of a patterned wafer before (a) and after (b) plasma exposure. (c) shows the surface-potential measurement (4×4 μm^2) after the wafer was exposed to UV radiation from a mercury-argon lamp.

before and after plasma exposure were made to assess the effects of aspect ratio on plasma charging.

In the past, surface-potential measurements were made with conventional Kelvin probes.[11] The spatial resolution of these probes is constrained by their tip dimensions (~2.5 mm diameter) which are too large to resolve the potential differences that can appear across narrow linewidth, high-aspect-ratio topographic structures. Spatial resolution of the potential inside as well as between the pit regions necessitates the use of specialized micro-Kelvin probes[12] or, as used in this work, scanning surface-potential microscopy (SSPM) using an atomic force microscope (AFM) as a Kelvin probe.

SSPM is a two-pass procedure where the surface topography is obtained in the first pass by operating the AFM in the intermittent-contact mode. Following this, the surface potential is measured by operating the AFM as a Kelvin probe. The topography and surface-potential measurements are interleaved. That is, they are each measured one line at a time with both images displayed simultaneously. A Digital Instruments Multimode® AFM with a Nanoscope IV controller[13] was operated as the SSPM system.

To further enhance the spatial resolution of the AFM beyond the standard AFM probe tip dimensions, a multiwalled carbon nanotube was attached to the apex of the Si AFM probe tip. This probe tip was purchased from Nanoscience Instruments and had a resonant frequency and force constant of ~70 kHz and 3.0 N/m, respectively. The nanotube was 1100–1200 nm in length and approximately 20 nm in diameter.

Using SSPM, no measurable change in surface potential was observed for an unpatterned wafer sample after plasma exposure. This indicates that the ion and electron fluxes were approximately equal at the outset over the unpatterned wafer surface and that the potential on the wafer surface was 0–1 V. However, for patterned wafers, a spatially averaged potential V_{av}, which was significantly larger than the surface potential of the unpatterned wafer, appeared at all locations on the wafer, *even on the flat unpatterned surfaces between the pits*.

The dependence of V_{av} on the aspect ratio (depth/diameter of the pit) of the structures is shown in Fig. 1. An aspect ratio of 0 in Fig. 1 corresponds to an unpatterned wafer. As seen in Fig. 1, V_{av} increases with aspect ratio for aspect ratios up to a value of 4:1. For aspect ratios greater than 4:1, the change in V_{av} as a function of aspect ratio is negligible.

In addition to the V_{av} measurements shown in Fig. 1, two-dimensional SSPM scans before and after plasma exposure were made for a structure with an aspect ratio of 1:1. These are shown in Fig. 2. V_{av} was subtracted from these

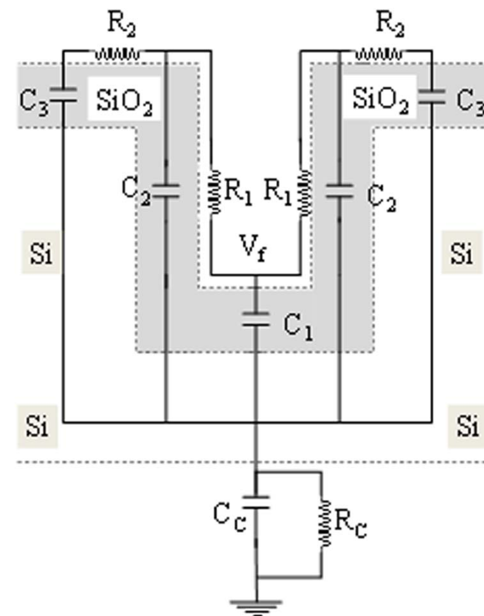

FIG. 3. (Color online) Equivalent-circuit model of a single high-aspect-ratio pit exposed to plasma.

measurements to examine the change in surface potential as a function of the surface topography.

Figure 2(a) shows that before plasma exposure, the surface potential inside the pit is very small (~10 mV). However, after plasma exposure, the surface potential inside the trench exceeded the potential at the top of the trench by approximately 200 mV. This is shown in Fig. 2(b).

The higher potentials seen inside the pit were not always present. This can be due to several factors. These are (1) deterioration of the carbon nanotube probe tip with time, (2) oxide surface currents,[14] and (3) measurement artifacts introduced by the deep pit sidewalls during the surface-potential scan.[15]

To ascertain that the measurement shown in Fig. 2(b) was not an artifact, the sample was exposed to UV radiation from a mercury-argon lamp, then the sample remained in the SSPM system. It was anticipated that UV radiation would inject electrons from the grounded Si substrate (photoinjection) and neutralize the plasma-deposited positive charge on the wafer.[16]

Remarkably, after ~15 s exposure to UV radiation, V_{av} dropped to the uncharged state that existed before the wafer was exposed to the plasma. In addition, as shown in Fig. 2(c), a decrease in the surface potential *inside* the holes was also measured after exposure of the plasma-charged wafer to UV radiation. The decrease in the wafer surface potential after UV exposure suggests that the higher potential inside the hole for the plasma-charged wafers is a real effect and not a measurement artifact.

The surface-potential measurements presented here show that an aspect-ratio-dependent surface potential V_{av} exists everywhere on the wafer surface after plasma exposure. Although the potential inside the pit was greater than V_{av} by approximately 0.2 V, it was much smaller in comparison to V_{av} (~3 V). We now present a circuit model that is consistent with existing electron and ion-shading theory[17,18] to explain the presence and AR dependency of V_{av}.

Figure 3 shows an equivalent-circuit representation of the pit structure during plasma exposure. The oxide layer is

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modeled as a group of capacitors $C_1 - C_3$. Capacitors C_1 and C_3 are equal, while C_2 depends on the depth of the pit. The surface conductivity of the oxide layer, assumed to be fairly low but not negligible,[19] is accounted for in the model by resistors R_1 and R_2. The bulk conductivity of the oxide layer is neglected since it is expected to be much smaller than the surface conductivity of the oxide.[20–22] The Si substrate is assumed to be an equipotential. In Fig. 3, C_C and R_C represent the capacitance and resistance introduced by the carbon tape that was used to secure the wafer chuck to the chamber.

We assume that the ion and electron currents reaching the unpatterned region on the wafer surface are approximately equal and that no charging beyond that observed in an unpatterned wafer occurs here. Hence, capacitors C_2 and C_3 are charged only to a potential of approximately 1 V. However, in accordance with electron-shading theory, we anticipate that the potential at the bottom of the pit will be much larger than this due to the imbalance between the ion and electron currents reaching the pit bottom. Thus, capacitor C_1 will charge to the potential V_f, which is approximated by[23]

$$V_f = V_P - \frac{T_e}{2} \ln\left(\frac{M}{2\pi m}\right) + T_e \ln\left(\frac{k_i}{k_e}\right), \tag{1}$$

where V_P (V) is the plasma potential, T_e (eV) is the electron temperature, m (kg) is the electron mass, and M (kg) is the ion mass. k_i and k_e are the ion and electron-shading parameters, respectively, and are defined as the ratio of the number of ions (or electrons) reaching the hole bottom to the number of ions (or electrons) reaching the unpatterned wafer surface in the absence of the surface features. k_i is usually assumed to be 1 for small aspect ratio ($<4:1$), while k_e lies in the range from 0 to 1 and decreases with increasing aspect ratio.

From Fig. 3, it is seen that capacitors C_2 and C_3 will also charge up to V_f through the surface conductances. This is consistent with our measurement of a high average surface potential appearing everywhere on the wafer surface.

Based on this simple model, we now consider the wafer surface potential as a function of aspect ratio. As the aspect ratio of the pits increases, the electron current reaching the pit bottom decreases while the ion current remains unaltered. The hole at the top of the pit thus serves as the orifice of an ion gun. Thus, Eq. (1) predicts that the potential V_f will increase with aspect ratio because k_e, the measure of the number of electrons reaching the pit bottom, decreases with increasing aspect ratio, while k_i and other parameters in Eq. (1) remain relatively constant. Consequently, C_1 and, hence, C_2 and C_3 are charged to a higher potential (V_f) with increasing aspect ratio. However, the surface potential increase with aspect ratio does not continue indefinitely. Figure 1 shows that the surface potential is constant for aspect ratios greater than 4:1. This phenomenon has been reported previously and is attributed to ion shading[3,18] which causes a reduction in the ion current reaching the pit bottom due to increased ion accumulation along the sidewalls of the pit with increasing aspect ratio.

In conclusion, we have shown that SSPM with carbon nanotube AFM tips can be used for direct measurement of the differential charging inside a high-aspect-ratio pit. The experimental results are consistent with the equivalent-circuit model presented here.

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