Vacuum-ultraviolet-induced charge depletion in plasma-charged patterned-dielectric wafers

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Plasma-induced charging of patterned-dielectric structures during device fabrication can cause structural and electrical damage to devices. In this work, we report on vacuum-ultraviolet (VUV) radiation-induced charge depletion in plasma-charged patterned-silicon-oxide dielectric wafers. Charge depletion is studied as a function of photon energy and the aspect ratio of hole structures. The wafers were charged in a plasma and subsequently exposed to monochromatic-synchrotron-VUV. Surface-potential measurements after VUV exposure showed that photon energies less than 11 eV were beneficial in depleting the plasma-induced charge from the patterned-dielectric wafers. In addition, for a given photon-flux density and for photon energies less than 11 eV, VUV-induced charge depletion *decreases* with increasing hole aspect ratio. The results are explained with a physically plausible equivalent-circuit model, which suggests that both electron photoinjection from Si into the oxide and oxide surface conductivity play an important role in the charge-depletion process. © 2009 American Institute of Physics. [DOI: 10.1063/1.3088889]

I. INTRODUCTION

Plasmas are used extensively in the semiconductor industry for film deposition, ashing, and etching of materials.[1] It is anticipated that, as technology progresses, the requirements for fabrication that involve plasma exposure will keep increasing.[2] However, plasma processing also has disadvantages. The plasma is a harsh environment since it contains high-energy electrons, ions, photons, and radicals that bombard the surface of the material to be processed. This can lead to charging of surfaces exposed to the plasma as well as charging of unexposed locations in the microstructure. In particular, during plasma etching, charging of the bottom or top edges of a high-aspect-ratio (depth/diameter) hole can alter the trajectories of the ions impinging on the material and etch the bottom corners of a pit/trench/hole (undercutting) thereby physically weakening the structure. Consequently, the overall yield as well as the reliability of semiconductor devices can be adversely affected.[2] As a result, controlling and mediating plasma-process-induced charging damage has become a crucial issue in assuring high process yields.

In this work, it will be shown that the plasma-induced charging of *patterned*-silicon-oxide dielectric wafers can be limited or completely neutralized by using vacuum-ultraviolet (VUV) radiation with photon energies less than 11 eV. In addition, using an equivalent-circuit model, we infer that both VUV-induced electron photoinjection from the Si substrate and the oxide surface conductivity play an important role in depleting the plasma-induced charge in patterned-dielectric wafers.

II. FABRICATION AND PLASMA CHARGING OF PATTERNED WAFERS

Here we present a description of the patterned-test structures used in this work and the plasma-charging methodology. The wafers used in this work are 100 mm in diameter Si wafers with 22 patterned dice. The dice have dimensions of 8×8 mm^2 as shown in Fig. 1(a). Each patterned die consists of holes that have a diameter of 0.8 μm with a hole spacing (pitch) of approximately 1.6 μm. The holes were fabricated on a bare-Si wafer by first etching into the Si using an HBr plasma. Holes were created with depths that varied from 1 to 11 μm, while keeping the hole diameter fixed, in order to study charging as a function of hole aspect ratio (AR). Following etching, a silicon-oxide layer was thermally grown on top of Si by wet oxidation at 1100 °C. The hole shown in Fig. 1(b) has a depth of 2 μm.

The entire patterned wafer with multiple dice, without cleaving, was exposed to a dc N$_2$ plasma discharge at 60 mtorr. A dc plasma was used instead of an rf plasma because
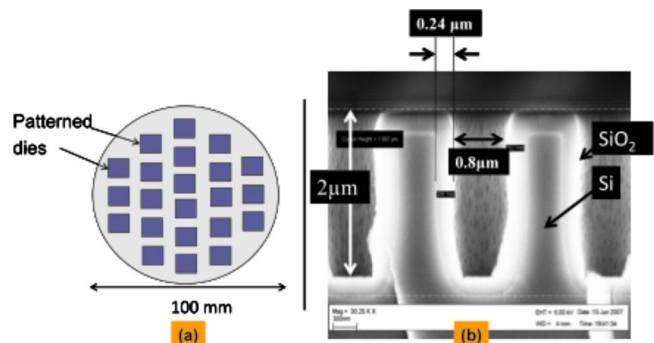

FIG. 1. (Color online) (a) Schematic of the 100 mm patterned wafer with 22 individual dice each with dimensions of $\sim 8 \times 8$ mm^2. (b) SEM image of the cross section of a sample patterned wafer with an AR of $\sim 2.5:1$.
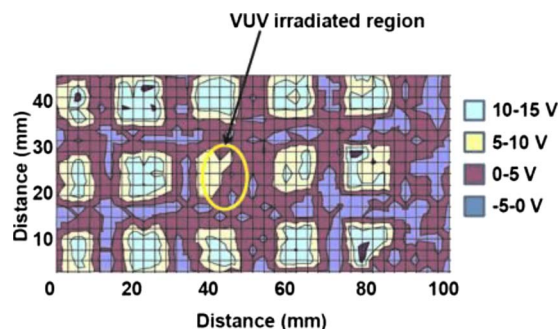
FIG. 2. (Color online) Surface-potential map of a 100 mm diameter patterned wafer exposed to 9 eV VUV radiation. The 2.5 mm resolution of the probe is interpolated by the software to create the map shown in the figure. The elliptical region in the figure shows the synchrotron beam size and location. The beam is peaked in the center.

the synchrotron facility restricted the use of rf sources. The dc plasma was generated by applying 400 V on the cathode, which was separated by ∼3 cm from the grounded anode. The patterned wafer was placed on the cathode and exposed to the plasma for ∼6 s. Kelvin-probe[3] measurements of the patterned wafer after plasma exposure indicated that, in the patterned regions of the wafer, it was charged up to large positive potentials (>15 V). Furthermore, the surface potential increased with AR of the holes in the patterned wafer, consistent with the electron-shading theory.[4] However, these potentials were beyond the measurement range of the Kelvin probe. In order to reduce the plasma-induced charging of the patterned dice to a measurable range, the plasma-charged patterned wafers were exposed to UV radiation ($h\nu$ =4.9 eV) from a Hg-Ar pen lamp with the lamp placed at a distance of ∼5 cm from the wafer surface. The UV-exposure time was adjusted so that the surface potential on the patterned dice was reduced to approximately 12 V for all samples prior to VUV exposure. The plasma-charged wafers were then exposed to VUV radiation with photon energies less than 11 eV at the University of Wisconsin-Synchrotron Radiation Center. Details about the VUV-exposure setup can be found in a previous publication.[5]

III. VUV EXPOSURE OF PLASMA-CHARGED PATTERNED WAFERS

A two-dimensional surface-potential map of a dc plasma-charged patterned wafer (rectangular hole AR of 2.5:1) as measured by a standard Kelvin probe (spatial resolution of ∼2.5 mm) is shown in Fig. 2. The patterned dice appear as islands of charge in the surface-potential map. The plotting software generates the smooth contours as shown in the figure by interpolation. The resolution of this probe is too large to resolve the potentials inside the holes, but we have previously used an atomic force microscope to find these potentials.[8] In this work, we are primarily concerned with the spatial potentials at the 2.5 mm resolution level.

The elliptical region in Fig. 2 was exposed to 9 eV VUV radiation with a time-integrated photon density of 7 $\times 10^{14}$ photons/cm^2 before the Kelvin-probe measurement was made. After plasma and subsequent UV exposure, as described above, Fig. 2 shows that the unpatterned regions

on the wafer (between the dice) were completely discharged while the potential in the patterned regions was ∼10–12 V for all dice *except* for the region that was exposed to VUV.

In this region, a significant decrease in surface potential is observed. In those dice immediately adjacent to the VUV-irradiated area, there are regions where the potential is 10–15 V, while in the VUV irradiated area only a minimum surface potential of ∼2.5 V was measured.

It must be noted that although UV photons are beneficial in depleting the plasma-induced charge, the charge-depletion efficiency for UV photons is significantly less than that for VUV radiation.[6] We experimentally verified that a significantly greater flux of UV photons is required to deplete the same amount of plasma-induced charge in the oxide as compared with VUV radiation (7–11 eV). The decrease in the charge-depletion efficiency for UV photons can be attributed to a decrease in the electron-photoinjection yield (defined as the ratio of the number of photoinjected electrons to the total number of photons incident on Si) from Si into the oxide as compared with the VUV photons.

The depletion dependence of the plasma-induced charge on photon energy of patterned-dielectric wafers was examined by exposing plasma-charged patterned wafers with a hole AR of 1.25:1 to VUV photon energies in the range from 8 to 11 eV. These energies were selected because significant depletion of the plasma-deposited charge has been observed at these photon energies for *unpatterned* oxide-coated Si wafers. The VUV-exposure system was aligned such that most of the VUV radiation was normally incident on a single patterned die on the wafer. A total time-integrated dose of 7 $\times 10^{14}$ photons/cm^2 was used for all VUV exposures. This dose was selected to ensure that the dielectric surface-potential reached its final steady-state value before the end of the VUV exposure. It was experimentally verified that exposing the samples for longer times did not produce any further decrease in the surface potential of the dielectric. Finally, the minimum surface potential in the region of VUV exposure of the patterned wafers was measured and is shown in Fig. 3(b) as a function of AR.

From Fig. 3(a), we observe that maximum charge depletion was obtained for irradiation with 8 eV photons. We also see that depletion is inversely proportional to photon energy and no measurable charge depletion was observed for 11 eV exposure of the plasma-charged patterned wafer. Subsequently, we develop an equivalent circuit model to indicate how this effect might take place.

VUV-induced charge depletion for a fixed photon flux was also measured as a function of AR of the holes in the patterned structure for four different photon energies and the results are shown in Fig. 3(b). Samples with ARs of 1.25:1, 2.5:1, and 3.75:1 were selected to study the dependence of charge depletion on AR. The experimentally measured surface potentials as a function of AR for four different photon energies are plotted in Fig. 3(b). Figure 3(b) shows that, with the exception of the 11 eV photons, for a fixed photon-flux density and photon energy, the measured surface potential is proportional to the AR.
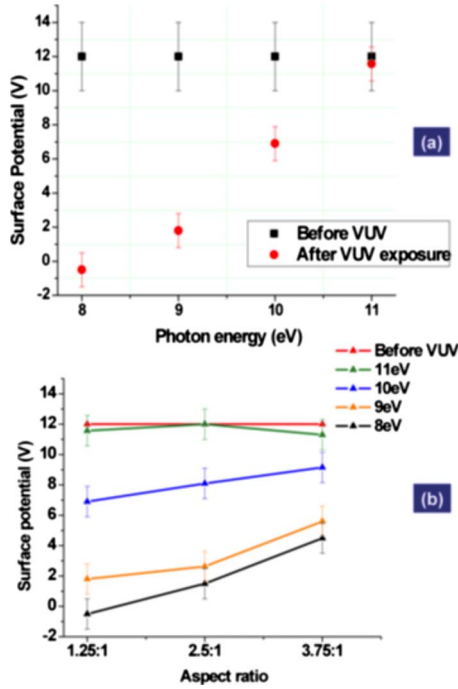
FIG. 3. (Color online) (a) Dependence of VUV-induced charge depletion in plasma-charged patterned wafers as a function of VUV photon energy for the same total photon flux. Note that the error bars shown in the graph above is representative of the measurement error introduced by the Kelvin probe. (b) VUV-induced charge depletion in patterned dielectric wafers as a function of AR for four different photon energies.

IV. EQUIVALENT-CIRCUIT MODEL

To help explain these results, an equivalent circuit was developed to model the VUV-radiation-induced charge depletion in the patterned dielectric wafers as a function of photon energy and AR. In particular, using the equivalent-circuit model, we can infer that the decrease in charge depletion with increasing photon energy can be due to (1) the decrease in electron photoinjection from Si into the oxide and (2) the increase in electron photoemission due to electron-hole pair creation in the oxide. Furthermore, we will also show that the decrease in charge depletion with increasing AR for a fixed photon flux and photon energy can be due to (1) the presence of a larger amount of plasma-induced charge along the hole sidewalls with increasing AR and (2) an increase in sidewall surface resistance with increasing AR.

Figure 4(a) shows the equivalent-circuit model for VUV exposure overlaid on a section of the patterned wafer. In Fig. 4(a), the oxide is represented by the capacitors C1, C2, and C3 along with the resistances indicated in regions A, B, and C of the figure, respectively. Photoemission due to electron-hole pair creation in the oxide and photoinjection from Si into the oxide (with subsequent photoemission into vacuum) are represented by the current sources I_{eh} and I_{pi}, respectively. The radiation-induced conductivity of the oxide layer due to electron-hole pair creation in the oxide as well as electron photoinjection from the silicon substrate into SiO_2 are represented by the resistors R_{eh} and R_{pi}, respectively. The surface resistance of the oxide layer is represented by the resistor R_s. Finally, the resistor R represents the current-return path through vacuum.
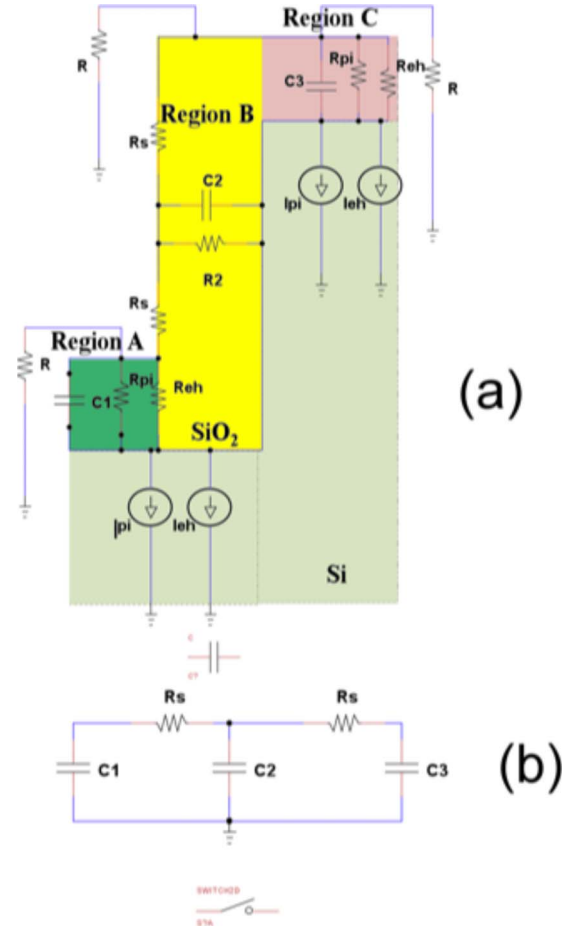

FIG. 4. (Color online) (a) Equivalent-circuit model for the patterned wafer during VUV exposure. (b) Equivalent-circuit model of the patterned wafer upon cessation of VUV irradiation.

After VUV exposure, the capacitors in Fig. 4(a) that represent the oxide can be charged to different potentials. To further investigate the behavior of the charge on the patterned wafer, a second equivalent-circuit model shown in Fig. 4(b) is used to represent the system after VUV exposure. The circuit of Fig. 4(b) suggests that, in the presence of a finite surface resistance, the voltage across the capacitors C1, C2, and C3 will equalize and reach a final steady-state value. At first glance, it appears that the voltages across the individual capacitors will fall to zero. This is not the case, since no current will flow through the resistances when the voltages across the capacitors are equal even if the individual capacitances are not equal.[7] This is consistent with our previous finding that the surface potentials everywhere on the wafer surface equalize to a steady-state potential after VUV exposure has ceased.[8] Since we are able to measure this steady-state voltage with the Kelvin probe, the calculated steady-state capacitor voltage in the model can be compared with the actual surface-potential measurements.

Next, the values of the individual circuit elements in Figs. 4(a) and 4(b) are estimated. In Fig. 4(a), three different regions (Regions A, B, and C) of the oxide layer are highlighted. In these regions, the oxide is represented by the parallel-plate capacitors C1, C2 and C3 (along with their appropriate resistances), respectively. The modeling of the

oxide layer with parallel-plate capacitors was justified by making electric-field calculations, which showed that the electric fields in Regions A, B, and C in Fig. 4(a) are very close to that of a parallel-plate capacitor with no fringing fields. Thus, we can represent the capacitors $C1$ and $C3$ as

$$C1 = C3 = \frac{A\varepsilon\varepsilon_0}{d}, \tag{1}$$

where A (m²) is the plate area, d (m) is the spacing between the two plates of the capacitor, and ε is the oxide relative permittivity. The plate area was determined from the dimensions of the hole bottom, which is circular with a radius of 0.4 μm. The area of this capacitor plate can then be computed as, $A = \pi \times (0.4\ \mu\text{m})^2 = 0.5 \times 10^{-12}$ m². d is set to the oxide thickness (240 nm). Finally, $\varepsilon = 3.9$ is the relative permittivity of silicon oxide. By substituting the values of A, d, and ε in Eq. (1), $C1$ and $C3$ were calculated to be $\sim$0.07 fF.

Next, although the sidewall capacitor $C2$ is also assumed to be a parallel-plate capacitor, the plate area for capacitor $C2$ is proportional to the depth of the hole. Thus, for the 1.25:1 AR sample with a hole depth of 1 μm and hole diameter of 0.8 μm, the plate area was estimated to be 0.8 $\times 10^{-12}$ m². The same plate area and the same values of ε and d were used as those for the capacitors $C1$ and $C3$. A value of 0.1 fF was calculated for capacitor $C2$ by using Eq. (1). With increasing hole depth, only the plate area of capacitor $C2$ changes, while the plate-separation distance given by the oxide thickness (240 nm) remains the same. Therefore, for the 2.5:1 AR sample with a hole depth of 2 μm, the plate area was 1.6×10^{-12} m², which leads to a capacitance of $\sim$0.2 fF. Finally for the 3.75:1 AR sample with a hole depth of 3 μm, the capacitance $C2$ was calculated to be $\sim$0.3 fF using the same method.

We now estimate the magnitudes of the current sources in the equivalent circuit of Fig. 4(a). To do this, we note that VUV exposure of oxide-coated wafers (thickness $\sim$200 nm) with photon energies less than 11 eV can cause (1) electron injection from Si into the oxide and subsequently into vacuum and/or (2) electron emission due to electron-hole pair creation in the oxide. Thus, electron photoinjection and photoemission by electron-hole pair creation in the oxide can be represented in the equivalent circuit by the constant current sources I_{pi} and I_{eh} as shown in Fig. 4(a).

Following previous work,[9] we can estimate the magnitudes of I_{pi} and I_{eh}. First, we note that the externally measured substrate current during the 8 eV VUV exposure is primarily due to photoinjection because the 8 eV photons do not possess enough energy to generate electron-hole pairs in the oxide. Consequently, we assume that I_{pi} *decreases* exponentially with increasing photon energy. We use the exponential photoinjection-decay constant as a fitting parameter. Similarly, I_{eh} was estimated by assuming that the substrate current measured at 11 eV is caused *primarily* by electron photoemission from electron-hole-pair creation in the oxide. Then, we assume that I_{eh} *increases* exponentially with photon energy with a separate exponential constant also used as a fitting parameter. The two exponents are not assumed to be equal. The fitted photoinjection and photoemission currents
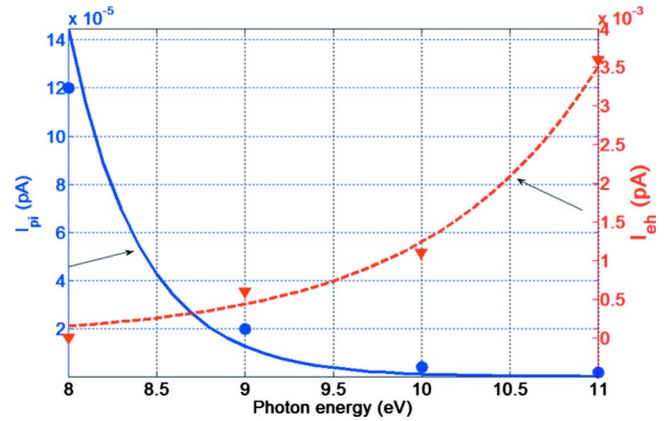

FIG. 5. (Color online) Photoinjection current (I_{pi}) and photoemission current (I_{eh}) due to electron-hole pair creation in the oxide as a function of photon energy.

as a function of photon energy are shown in Fig. 5 along with the experimental data.

We now proceed to estimate the surface and bulk resistances of the oxide layer in the three regions shown in the equivalent-circuit model. We begin by considering the resistor $R2$, which represents the resistance in region B of Fig. 4(a). We hypothesize that the conductivity in region B of Fig. 4(a) can only be increased by introducing electrons into this region. To determine $R2$ in Fig. 4(a), electric-field calculations were made by solving Laplace's equation for the potential inside the patterned wafer using finite differences. The calculations show that the electric field lines entering from the substrate boundary do not reach region B. Hence, we can assume that the bulk resistance of the oxide, $R2$, is a function of the oxide geometry only and is not affected by any VUV irradiation. Thus, $R2$ is assumed to be the intrinsic resistance of the oxide and can be determined by using the expression

$$R2 = \frac{\rho d}{A}, \tag{2}$$

where ρ (Ω m) is the intrinsic resistivity of the oxide, d (m) is the oxide thickness, and A (m²) is the area of the sidewalls. Thus for $A = 0.8 \times 10^{-12}$ m², $d = 240$ nm and $\rho = 10^{16}$ Ω m, $R2$ was estimated to be $\sim 3 \times 10^{21}$ Ω.

The surface resistance R_s of the oxide layer is difficult to estimate accurately as it is strongly influenced by impurities in the oxide, imperfections near the oxide surface, as well as atmospheric pressure and humidity. Therefore, the resistor R_s was also used as a fitting parameter. We assume that the surface resistance increases linearly with the hole depth because, as the hole becomes deeper, the electrons have to travel a greater distance along the hole sidewalls before they can neutralize the plasma-deposited charge. In addition, we propose that R_s is independent of the VUV photon energy and is not significantly influenced by electron injection from the Si in regions A and C into the oxide. This is the case because, under these assumptions, the photoinjected electrons cannot reach region B in Fig. 4(a) due to the presence of the fringing electric fields in the oxide.

Finally, we examine the VUV radiation-induced conductivity in regions A and C of the patterned structure. During
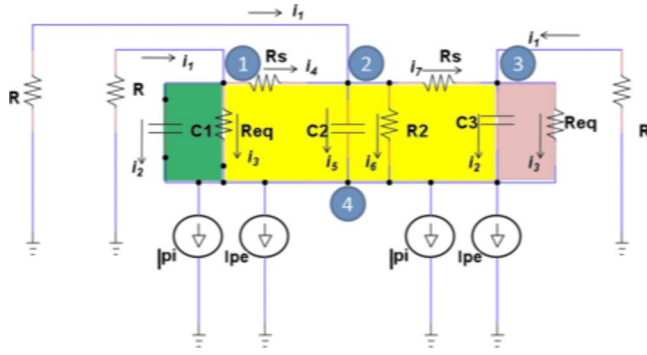
FIG. 6. (Color online) Redrawn equivalent circuit of Fig. 4(a) to determine the circuit equations at nodes 1–4.

VUV radiation, with photon energies less than 11 eV, the conductivity of the oxide layers in regions A and C of Fig. 4(a) can increase due to the introduction of free-charge carriers in the oxide either by electron photoinjection from the Si or by electron-hole pair creation in the oxide. Thus, we infer that the conductivity of the oxide is a function of the photoinjection and photoemission currents. Therefore, the resistances R_{pi} and R_{eh} are modeled to be inversely proportional to I_{pi} and I_{eh} respectively. Hence,

$$R_{pi} = \frac{K1}{I_{pi}}, \tag{3}$$

$$R_{eh} = \frac{K2}{I_{eh}}, \tag{4}$$

where $K1$ and $K2$ are constants of proportionality and are used as fitting parameters in the model. Note that, for the equivalent-circuit models shown in Figs. 4(a) and 4(b), the resistors R_{pi} and R_{eh} are the only circuit elements that depend on photon energy. In addition, the capacitor $C2$, representing the sidewall capacitance, and the resistor R_s that represents the surface resistance are the only circuit components that are a function of the hole AR.

V. CIRCUIT EQUATIONS

The equivalent-circuit model of Fig. 4(a) (valid *during* VUV exposure) is redrawn in Fig. 6 with the addition of voltages at nodes 1, 2, 3, and 4, which are V_1, V_2, V_3, and V_4 respectively. In addition, $R_{pi} \| R_{eh} = R_{eq}$ and $2I_{pi} + 2I_{eh} = I$. The node equations at nodes 1, 2, 3, and 4 can now be written as

$$\frac{dV_1}{dt} = \frac{1}{C1}\left[\frac{-V_1}{R} + C1\frac{dV_4}{dt} - \frac{V_1 - V_4}{R_{eq}} - \frac{V_1 - V_2}{R_s} \right], \tag{5}$$

$$\frac{dV_2}{dt} = \frac{1}{C2}\left[-\frac{V_2}{R} + \frac{V_1 - V_2}{R_s} + C2\frac{dV_4}{dt} - \frac{V_2 - V_4}{R2} - \frac{V_2 - V_3}{R_s} \right], \tag{6}$$

$$\frac{dV_3}{dt} = \frac{1}{C3}\left[\frac{V_2 - V_3}{R_s} + C3\frac{dV_4}{dt} - \frac{V_3}{R} - \frac{V_3 - V_4}{R_{eq}} \right], \tag{7}$$

$$2C1\frac{dV_1}{dt} - 2C1\frac{dV_4}{dt} + \frac{2(V_1 - V_4)}{R_{eq}} - C2\frac{dV_2}{dt} - C2\frac{dV_4}{dt}$$
$$+ \frac{V_2 - V_4}{R2} - I = 0. \tag{8}$$

Equations (5)–(8) can be solved for the node voltages V_1, V_2, V_3, and V_4 using the resistor, capacitor, and current values listed earlier. We further note that $(V_1 - V_4)$, $(V_2 - V_4)$, and $(V_3 - V_4)$ represent the voltages across the capacitors $C1$, $C2$, and $C3$, respectively. Equations (5)–(8) were solved using the initial conditions $V(C1) = V(C2) = V(C3) = 12$ V, which is the measured surface potential on the oxide produced by plasma exposure. The potentials were allowed to evolve with time and the calculation was terminated after $t = 1800$ s, which is a typical VUV exposure time for the plasma-charged patterned wafers.

As will be shown shortly, for particular VUV irradiation conditions and the smallest AR (1.25:1) used in this work, the model shows that all capacitors reach a constant, but not equal, potential at the end of the 1800 s VUV irradiation period. The potential values at the end of the 1800 s irradiation period for the lowest AR sample are referred to as $V_{1800,j}$, where j is an integer that identifies a particular capacitor. Under other VUV irradiation conditions, the capacitors might not reach a constant voltage at the end of the VUV irradiation period. However, as explained earlier, irrespective of the what the capacitor voltages at the end of irradiation might be, they will equalize after VUV radiation has ceased and yield a final steady-state voltage, which we refer to as V_{FINAL}. V_{FINAL} is the voltage that we measure experimentally with the Kelvin probe.

To model this behavior. the capacitor voltages, $V(C1)$, $V(C2)$, and $V(C3)$, at the end of VUV irradiation were used as the initial conditions for the equivalent circuit of Fig. 4(b) (valid *after* VUV exposure). The circuit of Fig. 4(b) suggests that in the presence of a finite surface resistance, the voltage across the capacitors $C1$, $C2$, and $C3$ will equalize and reach the final-state value V_{FINAL}. The capacitor voltages for the circuit in Fig. 4(b) can be found as follows:

$$V(C1) = V1(0) - \frac{1}{C1}\int_0^t I_a dt, \tag{9}$$

$$V(C2) = V2(0) - \frac{1}{C2}\int_0^t (I_a - I_b)dt, \tag{10}$$

$$V(C3) = V3(0) - \frac{1}{C3}\int_0^t I_b dt. \tag{11}$$

In Eqs. (9)–(11), $V1(0)$, $V2(0)$, and $V3(0)$ are the voltages on the capacitors $C1$, $C2$, and $C3$ at the end of the VUV-irradiation period. The surface resistances permit charge to flow between the capacitors and equalize in steady state. Thus, $V(C1) = V(C2) = V(C3) = V_{FINAL}$.

VI. ESTIMATION OF FITTING PARAMETERS

Here we describe the fitting process that was used to fit the model to the experimental surface-potential data shown

in Fig. 3(a). Note that there are five fitting parameters in the equivalent-circuit model. They are (1) the photoinjection current (I_{pi}), (2) the photoemission current induced by electron-hole pair creation in the oxide (I_{eh}), (3) the photoinjection-induced conductivity ($K1/I_{\text{pi}}$), (4) the electron-hole-pair induced conductivity ($K2/I_{\text{eh}}$), and (5) the oxide surface resistance (R_s).

Recall that for the photon-energy dependence experiments, the VUV irradiation time was chosen to be long enough so that no further depletion in charge was measured with VUV irradiation times longer than 1800 s for the 1.25:1 AR sample. Hence, in this case, $V_{1800}=V_{\text{FINAL}}$, which is the experimentally measured surface potential.

We first consider 8 eV photons. For these photons, the two fitting parameters, I_{pi} and I_{eh}, can be eliminated. This is because at 8 eV, I_{pi} can be determined directly from the experimental substrate-current value, since we assumed that photoemission due to electron-hole pair creation in the oxide is negligible for 8 eV photons. Under this assumption, the measured substrate current would entirely be due to photoinjection. Thus I_{eh}, the photoemission current due to electron-hole pair creation in the oxide, is set to zero. In addition, at 8 eV, the value of $K2$ can be set to zero because the resistance R_{eh} is infinite since I_{eh} was set to zero for this photon energy. Consequently, for 8 eV photons, only two fitting parameters ($K1$ and R_s) remain to be determined.

$K1$, and hence R_{pi}, is the parameter that effects the capacitor discharge time and also the final steady-state potential (V_{1800} or V_{FINAL}) for the capacitors $C1$ and $C3$ in the equivalent circuit of Fig. 4(a) for 8 eV photons. Note that the potential of $C1$ and $C3$ at the end of irradiation in the circuit of Fig. 4(a) is a function of the *charging* current, the capacitance, and the charge-decay time. Increasing $K1$ causes the charge-decay time and the final steady-state potential of capacitors $C1$ and $C3$ to increase, while decreasing $K1$ causes the voltage on the capacitors $C1$ and $C3$ to decay more rapidly and thus reach a lower steady-state potential. Thus, the value of $K1$ can be determined, based on these considerations, by solving Eqs. (5)–(11) for the capacitor voltages $V(C1)$ and $V(C2)$ and choosing that value of $K1$, which results in the capacitor potentials matching the experimentally measured steady-state potential at 8 eV. The fitting of $K1$ is independent of R_s since the capacitors $C1$ and $C3$ do not discharge through R_s.

Next, we determine the value of R_s, the sidewall surface resistance. R_s determines the rate at which the capacitor $C2$ decays. Therefore, after $K1$ was determined, R_s was chosen such that the capacitor voltage on $C2$ reached the experimentally determined steady-state potential after 1800 s, which again is the time after which the experimental measurements showed no further change in surface potential. The calculated time evolution of the capacitor voltages V_{C1}, V_{C2}, and V_{C3} for the 8 eV exposure of the 1.25:1 AR structure is shown in Fig. 7. Note that the steady-state potential as measured by the Kelvin probe many hours after exposure does change for VUV exposure times longer than 1800 s.

In order to determine $K2$, we look at the 11 eV exposures. For these exposures, I_{eh} was assumed to be entirely due to the experimentally measured substrate current. This is
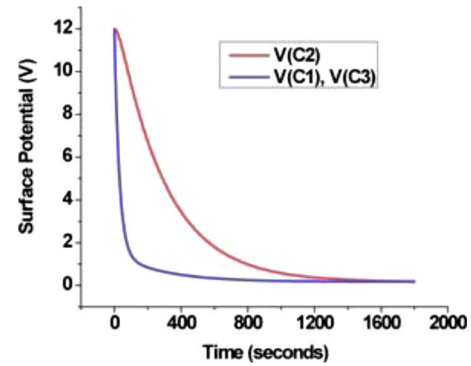

FIG. 7. (Color online) Time evolution of the capacitor potentials during 8 eV VUV irradiation of a plasma-charged patterned wafer with an AR of 1.25:1.

because we assumed that the substrate current is entirely due to photoemission by electron-hole-pair creation at this photon energy. In addition, I_{pi} was set to zero since photoinjection from Si can be neglected at 11 eV because the 11 eV photons cannot penetrate the 240 nm thick oxide layer.[10] Hence for the 11 eV case, there is no dependence of the capacitor potentials V_{C1}, V_{C2}, and V_{C3} on $K1$, since I_{pi} was set to zero. Thus, the value of $K3$, which caused capacitors $C1$ and $C3$ to reach the experimentally measured steady-state potential for the 11-eV exposures, was selected by solving Eqs. (5)–(11). It was found that values of 0.01 V, 0.1 V, and 0.7×10^{19} Ω for $K1$, $K2$, and R_s, respectively, fit the experimental surface-potential data for *both* the 8 and 11 eV exposures.

Following the determination of the fitting parameters $K1$, $K2$, and R_s, we consider the 9 and 10 eV exposures. To allow the model to fit the data, as previously discussed, I_{pi} was assumed to exponentially decrease with increasing photon energy, while I_{eh} was assumed to exponentially increase with photon energy. Values of I_{pi} and I_{eh} were found that yielded a good fit with the experimental surface-potential data shown in Fig. 3(a) for these exposures. The values of I_{pi} and I_{eh} obtained from this fitting process were used to determine the exponential constants (see Fig. 5) for these currents as a function of photon energy. Thus, the five fitting parameters are now determined.

The final steady-state potential ($V_{1800}=V_{\text{FINAL}}$) across the capacitors as a function of photon energy is shown in Fig. 8 for the 1.25:1 AR sample. The experimental measurements of the surface potential are also shown in the same graph. The good fit of the experimental data to the modeling results helps validate the two parts of our hypothesis. First, the decrease in charge depletion with increasing photon energy is due to a decrease in electron photoinjection. Second, the increase in electron photoemission with increasing photon energy is due to electron-hole pair creation in the oxide. Recall that electron photoemission is caused by photon-induced electron-hole pair creation in the oxide with subsequent emission of electrons from the dielectric into vacuum.

We now proceed to use these fitting parameters to show that the model also satisfactorily explains VUV-induced charge depletion as a function of the hole AR for a fixed photon energy and photon flux.
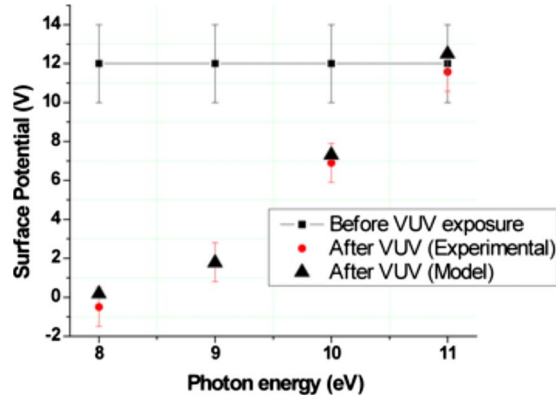
FIG. 8. (Color online) Simulation and experimental results for VUV-induced charge depletion in patterned wafers as a function of photon energy.

VII. EXTENSION OF RESULTS TO HIGHER ASPECT RATIOS

Here, we extend the model to the 2.5:1 and 3.75:1 AR cases. Recall that both the sidewall capacitance ($C2$) and the surface resistance (R_s) are strongly dependent on the hole geometry and are assumed to be the only circuit elements that are influenced by the AR. Thus, by scaling $C2$ and R_s as a function of the hole depth and by using the fitting parameters determined previously in Sec. VI, we can use the model to estimate the capacitor voltages, V_{C1}, V_{C2}, and V_{C3}, at the end of VUV radiation exposure for samples with ARs of 2.5:1 and 3.75:1.

The time evolution of the capacitor voltages (as determined by the model) is shown in Fig. 9 for a patterned wafer with an AR of 3.75:1 irradiated with 8 eV photons. From Fig. 9, it can be seen that (in contrast with Fig. 7 for the 1.25:1 AR sample) the voltages on the capacitors $C1$ and $C3$ rapidly decay to their steady-state value ($\sim$0.2 V) while capacitor $C2$ is only discharged to $\sim$7 V at the end of the irradiation period. Thus, unlike that of the 1.25:1 AR sample, $V_{1800} \neq V_{FINAL}$. The larger value of V_{C2} as compared to V_{C1} and V_{C3} at the end of the VUV irradiation period is justified for the following reasons.

Recall that after plasma charging, charges are distributed everywhere on the wafer surface including the sidewalls.[8] Furthermore, the shading of photons due to the hole geometry causes fewer photons to reach the sidewalls than the top
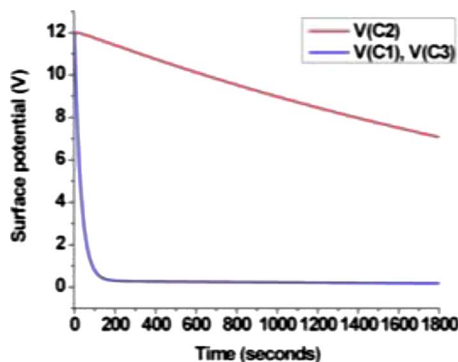

FIG. 9. (Color online) Time evolution of the capacitor potentials during 8 eV VUV irradiation of a plasma-charged patterned wafer with an AR of 3.75:1.
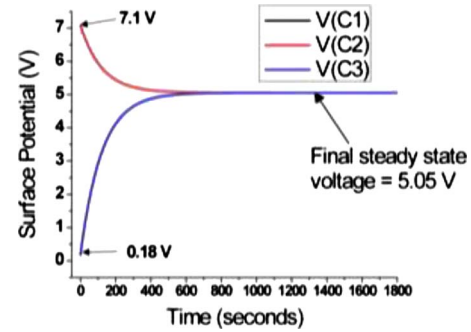

FIG. 10. (Color online) Calculated result showing the equalization of potentials on all capacitors in the patterned dielectric with AR of 3.45:1 after 8 eV VUV radiation.

or bottom of the hole due to the collimated nature of the VUV beam. Thus, it follows that $C2$, which models the hole sidewall, would be discharged to a lesser extent than $C1$ or $C3$ as fewer photoinjected electrons are available in this region to neutralize the plasma-deposited surface charge.

The capacitor voltages V_{C1}, V_{C2}, and V_{C3} were used as input parameters in the equivalent circuit of Fig. 4(b) and the computed final steady-state voltage (V_{FINAL}) was computed and compared with the experimental surface-potential measurement. Figure 10 shows the equalization of voltages across the three capacitors for the case of the 3.75:1 AR wafer subjected to 8 eV VUV radiation. The calculated steady-state capacitor voltage (V_{FINAL}) of $\sim$5 V compares favorably with the experimental measurement of 4.7 V.

The capacitor voltages at the end of the 8 eV VUV-irradiation period for patterned wafers are listed as a function of AR in Table I along with the computed steady-state capacitor voltages (V_{FINAL}) and the experimental final steady state surface-potential values. The same calculations were made for the cases of 9, 10, and 11 eV exposures for the three ARs investigated in this work. The modeling results (final steady-state capacitor voltage) of the AR dependence of VUV-induced charge depletion for the 8, 9, 10, and 11 eV VUV exposures are shown in Fig. 11.

Note from Table I that the 8 eV VUV exposure of the 1.25:1 sample yields a negative measured surface potential that is most likely due to measurement error associated with the Kelvin-probe system. The error was estimated by applying a fixed voltage across a capacitor and monitoring the Kelvin-probe output and is within 500 mV for potentials less than 10 V.

The modeling results shown in Fig. 11 indicate that VUV-induced charge depletion *decreases* with increasing AR

TABLE I. Approximate calculated voltages across capacitors $C1$, $C2$, and $C3$ at the end of 8 eV VUV irradiation. Also shown are the calculated final steady-state voltage and experimentally determined surface potential.

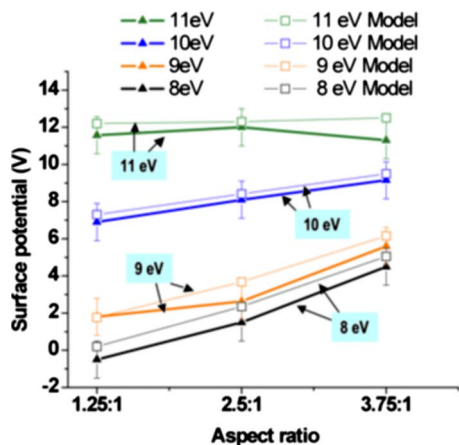| AR	V_{C1} (V)	V_{C2} (V)	V_{C3} (V)	V_{FINAL} (V)	Measured surface potential (V)
1.25:1	0.2	0.2	0.2	0.2	−0.4
2.5:1	0.2	3	0.2	2	1.7
3.75:1	0.2	7	0.2	5	4.7

FIG. 11. (Color online) VUV-induced charge depletion in patterned dielectric wafers as a function of AR for four photon energies.

for a fixed photon energy and photon flux and is in good agreement with the experimental measurements shown earlier in Fig. 3(b). This further validates the equivalent-circuit model.

VIII. INTERPRETATION OF ASPECT-RATIO DEPENDENCE OF VUV-INDUCED CHARGE DEPLETION

A potential explanation for the VUV-induced charge depletion as a function of the AR of the holes is now presented. First, we note that all the capacitors in the equivalent-circuit model are charged to the same initial voltage after plasma exposure. Hence, it follows that the total charge along the sidewalls, represented by the potential on capacitor $C2$, must increase with increasing capacitance for the same potential across that capacitor. Since $C2$ increases with hole AR, the amount of charge along the hole sidewalls also increases with AR to maintain the same potential across the capacitor. The increase in the charge on the hole sidewalls with increasing AR suggests that, for a given photon energy, more photoinjected electrons are required to neutralize the charging along the sidewalls because there are now more positive charges on the sidewall. Consequently, for a fixed photon flux and photon energy, the decrease in surface potential could be less for higher hole ARs.

In addition to the increase in charge along the hole sidewalls with AR, another quantity that causes a decrease in charge depletion with increasing AR is the surface resistance of the oxide. In order to determine the impact of the increase in surface resistance on charge depletion, we need to examine the mechanism by which the plasma-deposited positive charges along the sidewalls are neutralized. Neutralization of the plasma-deposited charge along the hole sidewalls can occur by transport of the photoinjected electrons to the sidewalls where they neutralize the positive charge remaining from plasma exposure.

Then, during VUV exposure, the photoinjected electrons could reach the wafer surface and subsequently move along the sidewalls where they neutralize the plasma-deposited positive charge. Thus, as the hole depth, and hence the AR, increases, the electrons must travel a longer distance to neu-

tralize the plasma charge. However, during their transit, the electrons can lose energy by scattering from the dielectric atoms. Thus, the probability that the electrons will reach the plasma-deposited charge and neutralize it decreases with increasing AR since the electrons might not possess sufficient energy to reach the plasma charge because of scattering losses and trapping. We therefore conjecture that, in addition to the increase in charging along the hole sidewalls, the increase in surface resistance with AR is also responsible for the reduction in charge depletion with increasing AR.

Finally, we consider why the decrease in surface potential with increasing AR is smaller for higher photon energies. At lower photon energies (8–9 eV), almost all of the incident photons reach the Si substrate and can increase the dielectric conductivity in regions A and C in Fig. 8 by injecting electrons into the oxide. In this case, the VUV-induced depletion can be limited by the increased charging and surface resistance of the oxide sidewalls as explained previously. For increasing VUV photon energy, the number of photoinjected electrons that are available to neutralize the plasma charge decreases. However, the sidewall surface resistance would not be significantly influenced by the increase in photon energy. Consequently, this implies that, for the higher photon energies, charge depletion can be limited by the number of photoinjected electrons that are available to deplete the plasma-deposited charge, thereby causing a reduction in the depletion yield with increasing photon energy.

IX. SUMMARY

We evaluated the feasibility of using VUV radiation to deplete the plasma-induced charge in patterned, oxide-coated wafers. Surface-potential measurements on plasma-charged patterned silicon oxide dielectrics after VUV exposure clearly showed that photon energies less than 11 eV are beneficial in depleting the plasma-induced charge in the dielectric. Experimentally, it was determined that VUV-induced charge depletion decreases with increasing AR of the holes for a given photon energy and photon flux. In order to help understand the results, equivalent-circuit models were developed for the patterned wafers. Similar to the case of the unpatterned wafers, it was determined that the electron photoinjection was the primary mechanism responsible for VUV-induced charge depletion in plasma-charged patterned oxide-coated wafers. Furthermore, it was determined that an increase in the charging along the hole sidewalls as well as the increase in surface resistance with AR can be responsible for the decrease in VUV-charge depletion with increasing AR of the samples.

ACKNOWLEDGMENTS

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